DATA PROCESSOR

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Inventor(s): KANEKO SUSUMU; KURAKAZU KEIICHI
Applicant(s): HITACHI LTD
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Abstract of **JP 1096747 (A)**

PURPOSE:To avoid the read of data in a user state and to recover the broken data when an exception is processed by securing such a condition where a CPU uses a RAM in a supervisor state and holds the data after setting an access inhibiting state at a newly set flag or a register. CONSTITUTION:A microprocessor is set under an access usable state when an access level designating bit is set at '1' in a control register MCR. Then an address in an address space of a built-in RAM 11 is delivered onto an address bus 21 in case the bit S/U of a status register is set at '0' in a CPU and in user state. At the same time, a coincidence signal C is delivered from an address comparing circuit 17. Thus, the output of AND gates G1 and G2 are set at H levels. These output signals are supplied to an exception processing circuit 8 as the access violation signals AV.